

CLAIMS

What is claimed is:

- 1 1. A comparator comprising:
2 a first input transistor with a first terminal, a second terminal and a gate terminal,
3 wherein the gate terminal is in communication with a first input and the first terminal of
4 the first input transistor is in communication with a first reference voltage via a first
5 electrical path, the first electrical path including a current source and a resistor to
6 generate a hysteresis offset;
7 a second input transistor with a first terminal, a second terminal and a gate
8 terminal, wherein the gate terminal is in communication with a second input and the first
9 terminal of the second input transistor is in communication with the first reference
10 voltage via a second electrical path, the first electrical path including a current source;
11 and
12 an output capable of setting toward the first reference voltage when a first signal
13 at the first input exceeds the hysteresis offset or a second reference voltage when the first
14 signal at the first input does not exceed the hysteresis offset.
- 1 2. A comparator as in claim 1, wherein the hysteresis offset is controllable.
- 1 3. A comparator as in claim 2, wherein the amount of current generated by the
2 current source is controllable, thereby affecting the hysteresis offset.

1 4. A comparator as in claim 1, further comprising third transistor with a first
2 terminal, a second terminal and a gate terminal, wherein the gate terminal of the third
3 transistor is in communication with the first terminal of the first input transistor.

1 5. A comparator as in claim 4, wherein the first terminal of the third transistor is
2 in communication with the first reference voltage via a third electrical path, the third
3 electrical path including a current source.

1 6. A comparator as in claim 5, wherein the output of the comparator is located
2 along the third electrical path between the first terminal of the third transistor and the
3 current source.

1 7. A comparator as in claim 1, wherein the gate of the third transistor is also in
2 communication with a fourth electrical path, the fourth electrical path including a
3 capacitor.

1 8. A comparator as in claim 7, wherein the fourth electrical path includes a
2 switch.

1 9. A device comprising:
2 a first programmable circuit operable to selectively provide a hysteresis offset in
3 response to a first programmable control signal; and
4 a comparator circuit, responsive to the first programmable circuit, to receive a
5 first and a second signals and compare the first signal and the second

6 signal with applying the hysteresis offset to the second signal, wherein the
7 comparator circuit provides a digital output signal in response to result of
8 comparison.

1 10. The device of claim 9 further comprising a second programmable circuit in
2 communication with the comparator circuit and operable to selectively provide a
3 hysteresis delay in response to a second programmable control signal, wherein the
4 comparator circuit compares the first signal and the second signal with applying the
5 hysteresis delay.

11. The device of claim 9, wherein the device is programmable by a user for
boundary-scan testing.

1 12. The device of claim 9, wherein the first and second input signals are mixed
2 signals.

1 13. The device of claim 9, wherein the first programmable circuit includes a
2 programmable impedance element for selectively setting the hysteresis offset in response
3 to a first programmable circuit control signal.

1 14. The device of claim 9, wherein the first programmable circuit includes a
2 programmable current source for selectively setting minimal voltage for input signals in
3 response to a first programmable circuit control signal .

1 15. The device of claim 14, wherein the programmable current source includes a
2 plurality of selectable current sources.

1 16. The device of claim 10, wherein the second programmable circuit includes
2 programmable capacitance element, wherein the programmable capacitance element
3 selectively sets hysteresis delay for input signals.

1 17. The device of claim 16, wherein the programmable capacitance element
2 includes a plurality of selectable capacitors and switchers, wherein the switchers is
3 operable to receive second programmable control signals.

1 18. The device of claim 9 further comprising a third programmable circuit in
2 communication with the comparator circuit and operable to selectively provide control of
3 magnitude of the digital output signal.

1 19. The device of claim 18, wherein the third programmable circuit further
2 includes a plurality of selectable current sources.

1 20. The device of claim 9, wherein further comprising a third programmable
2 circuit in communication with the first programmable circuit and operable to program an
3 output current source for facilitating the digital output signal.

1 21. A device comprising:
2 means for selectively providing a hysteresis offset in response to a first
3 programmable control signal;

4 means for receiving a first and a second signals; and
5 means for comparing the first signal and the second signal with applying the
6 hysteresis offset to the second signal, wherein the means for comparing
7 further includes means for providing a digital output signal in response to
8 result of comparison.

1 22. The device of claim 21 further comprising means for selectively providing a
2 hysteresis delay in response to a second programmable control signal, wherein the means
3 for comparing further includes means for comparing the first signal and the second signal
4 with applying the hysteresis delay the second signal.

1 23. The device of claim 21, wherein the device includes means for receiving
2 programmable information from a user for boundary-scan testing.

1 24. The device of claim 21, wherein the means for receiving a first and a second
2 signals further includes means for receiving mixed signals.

1 25. The device of claim 21, wherein the means for selectively providing a
2 hysteresis offset further includes means for selecting an impedance in response to the first
3 programmable circuit control signal.

1 26. The device of claim 21, wherein the means for selectively providing a
2 hysteresis offset further includes means for selectively providing a programmable current
3 source for setting minimal voltage for input signals in response to the first programmable
4 circuit control signal.

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1 27. The device of claim 26, wherein the means for providing a programmable
2 current source includes means for providing a plurality of selectable current sources.

1 28. The device of claim 22, wherein the means for selectively providing a
2 hysteresis delay further includes means for selectively setting capacitance in response to
3 the second programmable control signal.

1 29. The device of claim 28, wherein the means for selectively setting capacitance
2 further includes means for activating one capacitor or a combination of a plurality of
3 selectable capacitors.

1 30. The device of claim 21 further comprising means for selectively providing
2 control to magnitude of the digital output signal.

1 31. The device of claim 30, wherein the means for selectively providing control
2 to magnitude of the digital output signal includes means for selecting one current source
3 or a combination of a plurality of selectable current sources.

1 32. The device of claim 21 further comprising means for programming an output
2 current source for facilitating the digital output signal.

1 33. A method for a comparator comprising:
2 a) receiving first programmable control information;
3 b) setting a hysteresis offset in response to the first programmable control
4 information;
5 c) receiving a first and a second input signals;
6 d) offsetting the second input signal with the hysteresis offset; and

7 e) comparing the first input signal with the signal in step (d).

1 34. The method for claim 33 further comprising:
2 receiving second programmable control information;
3 setting a hysteresis delay in response to the second programmable control
4 information;
5 adjusting the second input signal in response to the hysteresis delay; and
6 comparing the first input signal with the adjusted second input signal.

1 35. The method of claim 33, wherein the method includes receiving first
2 programmable control information from a user.

1 36. The method of claim 33, wherein receiving a first and a second input signals
2 further includes receiving mixed signals.

1 37. The method of claim 33, wherein setting a hysteresis offset further includes
2 selecting an impedance in response to the first programmable circuit control signal.

1 38. The method of claim 33, wherein setting a hysteresis offset further includes
2 providing a programmable current source for selectively setting minimal voltage for input
3 signals in response to the first programmable circuit control signal .

1 39. The method of claim 38, wherein the a programmable current source includes
2 providing a plurality of selectable current sources.

1 40. The method of claim 34, wherein setting a hysteresis delay further includes
2 selectively setting capacitance in response to the second programmable control signal.

1 41. The method of claim 40, wherein the selectively setting capacitance further
2 includes activating one capacitor or a combination of a plurality of selectable capacitors.

1 42. The method of claim 33 further comprising selectively providing control to
2 magnitude of the digital output signal.

1 43. The method of claim 42, wherein the selectively providing control to
2 magnitude of the digital output signal includes selecting one current source or a
3 combination of a plurality of selectable current sources.

1 44. The method of claim 33 further comprising programming an output current
2 source for facilitating the digital output signal.

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1 45. A programmable comparator comprising:
2 a first programmable circuit operable to selectively provide a hysteresis delay in
3 response to a first programmable control signal; and
4 a comparator circuit, responsive to the first programmable circuit, to receive a
5 first and a second input signals in response to the hysteresis delay and
6 provide a digital output signal in response to result of comparison between
7 the first and second input signals

1 46. The programmable comparator of claim 45 further comprising a second
2 programmable circuit in communication with the comparator circuit and operable to
3 selectively provide a hysteresis offset in response to a second programmable control
4 signal, wherein the comparator circuit receives the first input signal and the second input
5 signal in response to the hysteresis offset.

1 47. The programmable comparator of claim 460, wherein the programmable
2 comparator is programmable by a user.

1 48. The programmable comparator of claim 45, wherein the first and second
2 input signals are mixed signals.

1 49. The programmable comparator of claim 46, wherein the second
2 programmable circuit includes a programmable impedance element for selectively setting
3 the hysteresis offset in response to a second programmable circuit control signal.

1 50. The programmable comparator of claim 46, wherein the second
2 programmable circuit includes a programmable current source for selectively setting
3 minimal voltage for input signals in response to a first programmable circuit control
4 signal .
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1 51. The programmable of claim 50, wherein the programmable current source
2 includes a plurality of selectable current sources.

1 52. The programmable comparator of claim 45, wherein the first programmable
2 circuit includes programmable capacitance element, wherein the programmable
3 capacitance element selectively sets the hysteresis delay for input signals.

1 53. The programmable comparator of claim 52, wherein the programmable
2 capacitance element includes a plurality of selectable capacitors and switchers, wherein
3 the switchers is operable to receive second programmable control signals.

1 54. The programmable comparator of claim 46 further comprising a third
2 programmable circuit in communication with the comparator circuit and operable to
3 selectively provide control to magnitude of the digital output signal.

1 55. The programmable comparator of claim 54, wherein the third programmable
2 circuit further includes a plurality of selectable current sources.

1 56. The programmable comparator of claim 46 further comprising a third
2 programmable circuit in communication with the comparator circuit and operable to
3 programming an output transistor for facilitating the digital output signal.

1 57. A programmable apparatus comprising:
2 means for selectively providing a hysteresis delay in response to a first
3 programmable control signal;
4 means for receiving a first and a second input signals in response to the hysteresis
5 delay; and
6 means for comparing the first and second input signals and providing a digital
7 output signal in response to result of comparison between the first and
8 second input signals.

1 58. The programmable apparatus of claim 57 further comprising means for
2 selectively providing a hysteresis offset in response to a second programmable control
3 signal, wherein the means for receiving a first and a second input signals further includes
4 means for receiving the first input signal and the second input signal in response to the
5 hysteresis offset.

1 59. The programmable apparatus of claim 58 further includes means for
2 receiving the first and second programmable control signals from a user.

1 60. The programmable apparatus of claim 57, wherein the means for receiving a
2 first and a second input signals further includes means for receiving mixed signals.

1 61. The programmable apparatus of claim 58, wherein means for selectively
2 providing a hysteresis offset includes means for selectively setting the hysteresis offset in
3 response to a second programmable circuit control signal.

1 62. The programmable apparatus of claim 58, wherein means for selectively
2 providing a hysteresis offset further includes means for selectively setting minimal
3 voltage for input signals in response to a first programmable circuit control signal.

1 63. The programmable apparatus of claim 62, wherein means for selectively
2 setting minimal voltage for input signals further includes means for providing a plurality
3 of selectable current sources.

1 64. The programmable apparatus of claim 57, wherein means for selectively
2 providing a hysteresis delay includes means for selectively setting capacitance in
3 response to the first programmable control signal.

1 65. The programmable apparatus of claim 64, wherein means for selectively
2 setting capacitance includes means for selecting one capacitor or a combination of a
3 plurality of selectable capacitors.

1 66. The programmable apparatus of claim 58 further comprising means for
2 selectively providing control to magnitude of the digital output signal.

1 67. The programmable apparatus of claim 66, wherein means for selectively
2 providing control to magnitude of the digital output signal further includes means for
3 selecting one current source or a combination of a plurality of selectable current sources.

1 68. The programmable apparatus of claim 58 further comprising means for
2 programming an output current source for facilitating the digital output signal.

1 69. A method for comparing input signals comprising:
2 a) providing a hysteresis delay in response to a first programmable control signal;
3 b) receiving a first and a second input signals in response to the hysteresis delay;
4 c) comparing the first and second input signals; and
5 d) providing a digital output signal in response to result of comparison between
6 the first and second input signals.

1 70. The method of claim 69 further comprising providing a hysteresis offset in
2 response to a second programmable control signal, wherein the receiving a first and a
3 second input signals further includes receiving the first input signal and the second input
4 signal in response to the hysteresis offset.

1 71. The method of claim 70 further includes receiving the first and second
2 programmable control signals from a user.

1 72. The method of claim 69, wherein the receiving a first and a second input
2 signals further includes receiving mixed signals.

1 73. The method of claim 70, wherein the selectively providing a hysteresis offset
2 includes selectively setting the hysteresis offset in response to a second programmable
3 circuit control signal.

1 74. The method of claim 70, wherein the selectively providing a hysteresis offset
2 further includes selectively setting minimal voltage for input signals in response to a first
3 programmable circuit control signal .

1 75. The method of claim 74, wherein the selectively setting minimal voltage for
2 input signals further includes providing a plurality of selectable current sources.

1 76. The method of claim 69, wherein the selectively providing a hysteresis delay
2 includes selectively setting capacitance in response to the first programmable control
3 signal.

1 77. The method of claim 76, wherein the selectively setting capacitance includes
2 selecting one capacitor or a combination of a plurality of selectable capacitors.

1 78. The method of claim 70 further comprising the selectively providing control
2 of magnitude of the digital output signal.

1 79. The method of claim 78, wherein the selectively providing control of
2 magnitude of the digital output signal further includes selecting one current source or a
3 combination of a plurality of selectable current sources.

1 80. The method of claim 70 further comprising programming an output current
2 source for facilitating the digital output signal.

1 81. A device comprising:
2 a first programmable circuit operable to selectively providing an output loading
3 on an output circuit in response to a first programmable control signal; and
4 a comparator circuit in communication with the first programmable circuit to
5 compare a first input signal and a second input signal and provide a digital
6 output signal in response to result of comparison and the output loading on
7 the output circuit.

1 82. The device of claim 81 further comprising a second programmable circuit
2 operable to selectively provide a hysteresis offset in response to a second programmable
3 control signal, wherein the comparator circuit receives the first and the second input
4 signals with applying the hysteresis offset.

1 83. The device of claim 81 further comprising a third programmable circuit in
2 communication with the comparator circuit and operable to selectively provide a
3 hysteresis delay in response to a third programmable control signal, wherein the
4 comparator circuit receives the first signal and the second signal with applying the
5 hysteresis delay.

1 84. The device of claim 81, wherein the device is programmable by a user.

1 85. The device of claim 81, wherein the first and second input signals are mixed
2 signals.

1 86. The device of claim 82, wherein the second programmable circuit includes a
2 programmable impedance element for selectively setting the hysteresis offset in response
3 to a first programmable circuit control signal.

1 87. The device of claim 82, wherein the second programmable circuit includes a
2 programmable current source for selectively setting minimal voltage for input signals in
3 response to a first programmable circuit control signal.

1 88. The device of claim 87, wherein the programmable current source includes a
2 plurality of selectable current sources.

1 89. The device of claim 83, wherein the third programmable circuit includes
2 programmable capacitance element, wherein the programmable capacitance element
3 selectively sets hysteresis delay for input signals.

1 90. The device of claim 89, wherein the programmable capacitance element
2 includes a plurality of selectable capacitors and switchers, wherein the switchers is
3 operable to receive second programmable control signals.

1 91. The device of claim 81, wherein the first programmable circuit selectively
2 controls magnitude of the digital output signal.

1 92. The device of claim 91, wherein the first programmable circuit further
2 includes a plurality of selectable current sources.

1 93. A device comprising:
2 means for selectively providing an output loading on an output circuit in response
3 to a first programmable control signal; and
4 means for comparing a first input signal and a second input signal and providing a
5 digital output signal in response to result of comparison and the output
6 loading on the output circuit.

1 94. The device of claim 93 further comprising means for selectively providing a
2 hysteresis offset in response to a second programmable control signal, wherein means for
3 comparing further includes means for receiving the first and the second input signals with
4 applying the hysteresis offset.

1 95. The device of claim 93 further comprising means for selectively providing a
2 hysteresis delay in response to a third programmable control signal, wherein means for
3 comparing further includes means for receiving the first signal and the second signal with
4 applying the hysteresis delay.
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1 96. The device of claim 93 further includes means for receiving the first, second
2 and third programmable control signals from a user.

1 97. The device of claim 93, wherein means for receiving the first and second
2 input signals further includes means for receiving mixed signals.

1 98. The device of claim 94, wherein means for selectively providing a hysteresis
2 offset further includes means for selectively providing an impedance for setting the
3 hysteresis offset in response to a first programmable circuit control signal.

1 99. The device of claim 94, wherein means for selectively providing a hysteresis
2 offset includes means for providing a programmable current source for selectively setting
3 minimal voltage for input signals.

1 100. The device of claim 99, wherein means for providing a programmable
2 current source includes means for providing a plurality of selectable current sources.

1 101. The device of claim 95, wherein means for selectively providing a hysteresis
2 delay further includes means for selectively setting capacitance in response to the third
3 programmable control signal.

1 102. The device of claim 101, wherein means for selectively setting capacitance
2 further includes means for activating one capacitor or a combination of a plurality of
3 selectable capacitors.

1 103. The device of claim 93, wherein means for selectively providing an output
2 loading further includes means for selectively controlling magnitude of the digital output
3 signal.

1 104. The device of claim 103, wherein means for selectively controlling
2 magnitude of the digital output signal includes means for selecting one or a combination
3 of a plurality of selectable current sources.

1 105. A method for performing a compare function comprising:
2 selectively providing an output loading on an output circuit in response to a first
3 programmable control signal; and
4 comparing a first input signal and a second input signal and providing a digital
5 output signal in response to result of comparison and the output loading on
6 the output circuit.

1 106. The method of claim 105 further comprising selectively providing a
2 hysteresis offset in response to a second programmable control signal, wherein the
3 comparing further includes receiving the first and the second input signals with applying
4 the hysteresis offset.

1 107. The method of claim 105 further comprising selectively providing a
2 hysteresis delay in response to a third programmable control signal, wherein the
3 comparing further includes receiving the first signal and the second signal with applying
4 the hysteresis delay.

1 108. The method of claim 105 further includes receiving the first, second and
2 third programmable control signals from a user.

1 109. The method of claim 105, wherein the receiving the first and second input
2 signals further includes receiving mixed signals.

1 110. The method of claim 106, wherein the selectively providing a hysteresis
2 offset further includes selectively providing an impedance for setting the hysteresis offset
3 in response to a first programmable circuit control signal.

1 111. The method of claim 106, wherein the selectively providing a hysteresis
2 offset includes providing a programmable current source for selectively setting minimal
3 voltage for input signals.

1 112. The method of claim 111, wherein the providing a programmable current
2 source further includes providing a plurality of selectable current sources.

1 113. The method of claim 107, wherein the selectively providing a hysteresis
2 delay further includes selectively setting capacitance in response to the third
3 programmable control signal.

1 114. The method of claim 113, wherein the selectively setting capacitance further
2 includes activating one capacitor or a combination of a plurality of selectable capacitors.

1 115. The method of claim 105, wherein the selectively providing an output
2 loading further includes selectively controlling magnitude of the digital output signal.

1 116. The method of claim 115, wherein the selectively controlling magnitude of
2 the digital output signal includes selecting one or a combination of a plurality of
3 selectable current sources.